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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,174	02/13/2004	Kenneth Koch II	10017911-3	4476
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HEWLETT-PACKARD COMPANY Intellectual Property Administration P.O. Box 272400 Fort Collins, CO 80527-2400			EXAMINER NGUYEN, LONG T	
			ART UNIT 2816	PAPER NUMBER

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/777,174

Applicant(s)

KOCH ET AL.

Examiner

Long Nguyen

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,7-12,14,16-18,20 and 21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,7-12,14,16-18,20 and 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/1/04 + 2/13/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: throughout the specification, references “28” and “30” are referred as “DC circuits”. However, it is not clear how the references “28” and “30” can be “DC circuits” because it appears from the drawings of Figure 1 that each of the “28” and “30” are just a path or a wire that connected. Further, it is also not clear how the “path” 28 and 30 can be “DC” because each of them has a voltage signal that transitions/swings between ground and supply Vdd which is not a DC voltage. Note that “DC path” and “DC connections” throughout the specification are also objected to for the similar reasons and because it is not clear what it means by “DC connections. Clarification and/or appropriate correction is required.

Claim Objections

2. Claims 1, 3, 7-12, 14, 16-18, 20 and 21 are objected to because of the following informalities:

Claim 1, line 11, “the circuitry” should be changed to --the pulse shaping circuitry-- for consistency.

Claim 1, line 12, it appears that “and capacitor” should be changed to --and a capacitor--

Claims 3 and 7-12 are objected to because they include the informality of claim 1.

Claim 14, line 11, “the circuitry” should be changed to --the pulse shaping circuitry-- for consistency.

Claims 16-18 are objected to because they include the informality of claim 14.

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Claim 20, line 8-9, "the circuitry" should be changed to --the pulse shaping circuitry-- for consistency.

Claim 21 is objected to because they include the informality of claim 20.

Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1, 3, 7-12, 14, 16-18, 20 and 21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6,753,708, claims 1-5 of U.S. Patent No. 6,759,880, and claims 1, 3-9, 11-24 of copending U.S. Application No. 10/777,902. Although the conflicting claims are not identical, they are not patentably distinct from each other because they claim substantially the same embodiment of the invention, i.e., all the claim limitations of U.S. Patents 6,753,708 and 6,759,880, and copending U.S. Application No. 10/777,902 anticipate all the claim limitations of the instant application.

Note that the double patenting with the copending U.S. Application No. 10/777,902 is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7-12, 14, 16-18, 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 7, “DC path” recited on lines 5 and 9 is indefinite because it is not clear how it is a “DC”. It is seen in the operation of the circuitry in Figure 1 that the path 28 having a voltage signal that transitions/swings between ground and power supply Vdd. It is suggested that “DC path” on lines 5 and 9 be changed to --direct connection path--.

Also, in claim 7, the recitation “the transistor” on line 6 lacks antecedent basis and it is not clear which transistor that the recitation refers to.

Also, in claim 7, “the first and second resistive element” on line 10 is indefinite because “the second resistive element” lacks antecedent basis and it is not clear where the second resistive element comes from.

Claims 8-12 are indefinite because they include the indefiniteness of claim 7.

Also in claim 9, the recitation “the field effect transistor” on line 4 lacks antecedent basis and it is not clear which transistor the recitation refers to.

Claims 8-12 are also indefinite because they include the indefiniteness of claim 9.

In claim 14, “DC connected” recited on lines 13 and 15 are indefinite because it is not clear it means by “DC” connected. Further, it is not clear how the first capacitor being DC connected between the control electrode of the first transistor and the first power supply

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terminal, and how the second capacitor being DC connected between the control electrode of the second transistor and the second power supply terminal. It appears that "DC connected" on lines 13 and 15 should be changed to --direct connected--.

Also in claim 14, "the first power supply terminal" on line 15 and "the second power supply terminal" on line 16 lack antecedent basis and it is not clear whether the first and second power supply terminals are of the opposite power supply terminals. Further, "a first power supply terminal" and "a second power supply terminal" on line 17 and 21 are unclear antecedent basis.

Claims 16-18 are indefinite because they include the indefiniteness of claim 14.

In claim 20, "DC connected" recited on lines 10 and 11 are indefinite for the similar reasons as discussed in claim 14. It appears that "DC connected" on lines 10 and 11 should be changed to --direct connected--.

Claim 21 is indefinite because they include the indefiniteness of claim 20.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3, 7-11, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Love (USP 5,068,553).

Note that Figure 3 of Love discloses a circuit which includes a first terminal (IN); a driver (86, 88) having a first transistor (PFET 86) and a second transistor (NFEF 88); output

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terminal (OUT); pulse shaping circuitry (68, 72, 70 and 80) comprising a resistive element (resistor 72), a capacitor (NFET 80) and a switching circuitry (68, 72, 70) comprising an inverter (68, 72, 70) wherein the inverter comprises the resistive element (resistor 72), a PFET (68) and an NFET (70). Note that because the PFET and NFET transistors having opposite conductivity so the on/off of transistors 86 and 88 in Figure 3 must be opposite to each other, i.e., transistors 86 and 88 are not ON simultaneously. Thus, because the structure of the claims are fully met so all the functional limitations of the claims are also met (MPEP 2114; In re Swinehart, 169 USPQ 226 (CCPA 1971); and In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997)).

9. Claims 14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamasaki et al. (USP 5,694,065).

Note that Figure 2 of the Hamasaki et al. reference discloses a circuit having an input terminal (IN); voltage source (INPUT signal); a driver (50, 60) comprising first and second opposite conductivity type transistors (PFET and NFET, respectively); opposite power supply terminals (Vdd and ground); an output terminal (OUT); a pulse shaping circuitry (70, 80); wherein the pulse shaping circuitry (70, 80) including: (a) first and second switching circuits (IV1- Rn, IV2- Rp) including output terminals (DO1 and DO2, respectively), and (b) first and second capacitors (Cn) and (Cp); a first power supply terminal (46), and a second power supply terminal (48); wherein the first switching circuit (IV1, Rn) comprises a first inverter (IV1, Rn) that includes third and fourth transistors (72 and 74) and also including the first resistive element (Rn); the second switching circuit (IV2, Rp) comprises a second inverter (IV2, Rp) that includes fifth and sixth transistors (82 and 84) and also including the second resistive element (Rp). Note that all the functional operations are met in the operation of the circuitry. Further, because the

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PFET and NFET transistors having opposite conductivity and because signals DO1 and DO2 having substantially same voltage level (i.e., signals DO1 and DO2 are inverted of input voltage signal IN), so the on/off of transistors 50 and 60 in Figure 2 must be opposite to each other, i.e., transistors 50 and 60 are not ON simultaneously. Thus, because the structure of the claims are fully met so all the functional limitations of the claims are also met (MPEP 2114; In re Swinehart, 169 USPQ 226 (CCPA 1971); and In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997)).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 1, 3, 7-12, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki et al. (USP 5,694,065) in view of Rapp (USP 5,280,420).

With respect to claims 1, 3 and 7-12, Figure 2 of the Hamasaki et al. reference discloses a circuit which includes a first terminal (IN); a driver (50, 60) having a first transistor (PFET 50) and a second transistor (NFET 60); output terminal (OUT); pulse shaping circuitry (72, 74, Rn, Cn, 82, 84, Rp and Cp) comprising a resistive element (resistor Rn), a capacitor (Cn) and a switching circuitry (72, 74) comprising an inverter (68, 72, 70). Note that, for broadest reasonable interpretation, the combination of elements 72, 74 and Rn forms an inverter, i.e., the output of inverter is signal DO1) wherein the inverter comprises the resistive element (resistor 72), a PFET (68) and an NFET (70). Figure 2 of the Hamasaki et al. reference does not disclose

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that the first capacitor (Cn) comprising a field effect device having a conductivity type opposite to the conductivity type of the first transistor (PFET 50). However, the Rapp reference discloses that a capacitor is formed by using an NMOS transistor that has its drain and its source connected together (lines 10-16 and lines 61-63 of Col. 7). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 2 of the Hamasaki reference to use specific capacitor-connected NMOS transistor (as taught by the by the Rapp reference) for broad capacitor elements in the circuit of Figure 2 of the Hamasaki reference (i.e., each of the capacitors Cn and Cp in Figure 2 is implemented by a capacitor-connected NMOS transistor) for the purpose of more efficiently implementation in silicon (see lines 10-16 of Col. 7 of Rapp) and therefore the operation of the circuitry would be more efficiency. Thus, this modification meets all the limitations of this claim including the “first capacitor comprising a field effect device having a conductivity type opposite to the conductivity type of said one of said transistors” because the capacitor Cn in this modification comprising an NMOS device (capacitor-connected NMOS transistor) having the conductivity opposite to the PMOS transistor (50). Note that all the functional limitations in this claim are also met because the structure of the claim is fully met as discussed above.

With respect to claims 17 and 18, the above modification as discussed in claims 1, 3 and 7-12 also meets all the limitations of these claims because the first and second capacitors are implemented by NMOS transistors so they comprise field effect transistors.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 1, 2004



Long Nguyen
Primary Examiner
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